Serie N° 5

The memories

Exercise 1

1. How many flip-flops are needed for MAR and MBR of 1K*4-bit memory?
2. How many words should a memory contain if its MAR is 8bits?
3. Using 256*4-bit RAM as a unit, design a memory of:
    a) 1 K*4 bits
    b) 1 K*8 bits.

Exercise 2

We have a machine whose address bus is 16 bits and the data bus is 8 bits. The memory of this machine consists of a RAM of 32Kilo*8 and a ROM of 16Kilo×8.1.

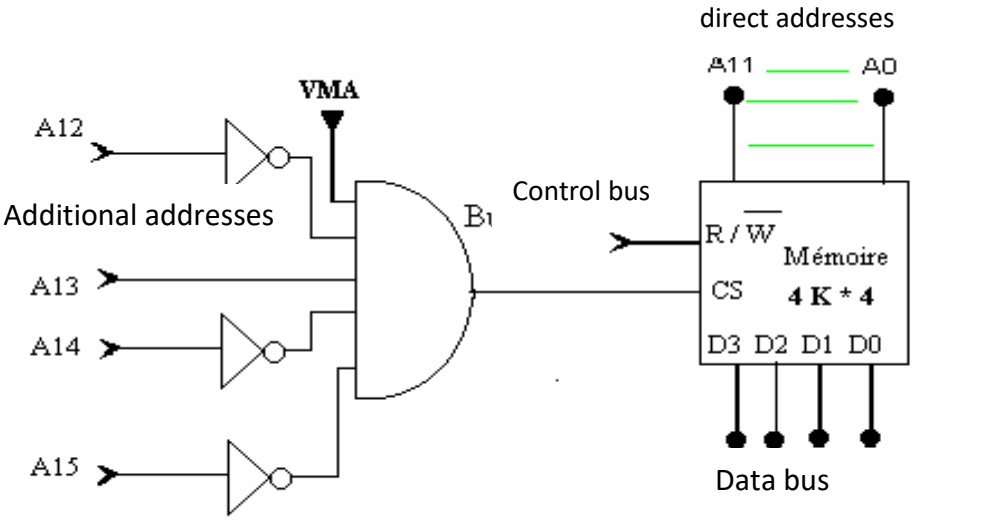
1. What are the sizes of the MAR and MBR address registers?

2. Give the functional diagram of this RAM using 32k×4bit memories

3. Give the complete functional diagram (RAM+ROM), indicating the addresses of each box.

Exercise 3

Consider a RAM memory of 4Kilos*4 represented by the following diagram:



1. What is the role of R/W and CS pins in a memory circuit.

2. How many bits make up the data stored in this memory?

3. What is the capacity of this memory (in Kbits and then in Kbytes).

4. What must be the state of the VMA (Valid Memory Access) signal and the state of lines A_{12} to A_{15} to select this memory.

5. Give the address range (in Hexadecimal) used by this memory.

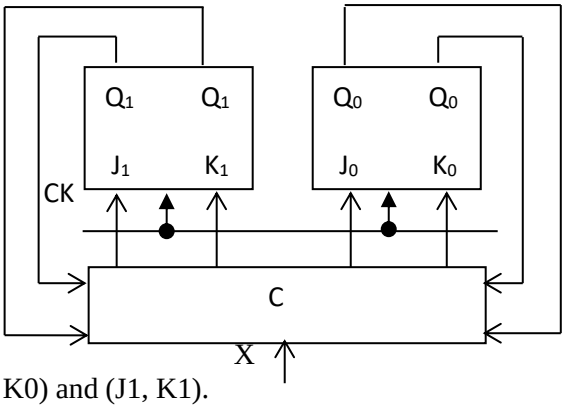
6. We want to increase the size of the data to 16bits by associating several 4K*4 memories, give the necessary connections.

Exercise 4 :

Consider a circuit defined by the operation and the following block diagram:

Q_1	Q_0	X	Q_1^+	Q_2^+
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

Functional diagram



1) Perform the circuit C allowing to give (J0, K0) and (J1, K1).

We want to achieve the same operation by using D flip-flops instead of JK flip-flops and a ROM memory instead of the C circuit.

2) Give the truth table and the new block diagram (specify the inputs and outputs). How many bits requested in the ROM?

Exercise 5

Establish the truth table of a 2-bit full adder.

Create the circuit of a 2-bit full adder using ROM.

Exercise 6

1- We consider a machine with the following configuration: a central memory of size 2 MØ, with memory words of 4 bytes and an address bus of size 20 bits.
2- 1- Calculate the minimum size of the address bus which allows this memory to be addressed.
3- 2- Determine the addressing range of this memory (minimum address and maximum address in Hex).
4- 3- In fact, this memory is made up of two separate blocks. The first is a RAM of 1 M bytes with words of 4 bytes addressable from address $(00000)_{16}$ and the second is a ROM of size 1 M bytes with words of 4 bytes addressable from the address $(60000)_{16}$.
5- a- Give the memory diagram showing the necessary connections.
6- b- Determine the two addressing ranges of RAM and ROM respectively. Is this computer's main memory expandable? If so, determine the size of the expansion memory and the minimum number of memory blocks (of the same size as the previous ones) that can be added? Justify your answer.